A 77 GHz 90 nm CMOS Transceiver for FMCW Radar Applications

Toshiya Mitomo, *Member, IEEE*, Naoko Ono, Hiroaki Hoshino, Yoshiaki Yoshihara, *Member, IEEE*, Osamu Watanabe, *Member, IEEE*, and Ichiro Seto, *Member, IEEE*

***Abstract*—The first 77 GHz frequency modulated continuous wave (FMCW) radar transceiver IC with an accurate FMCW chirp signal generator using a 90 nm CMOS process is presented. To realize accurate FMCW radar system in CMOS, a PLL synthesizer based FMCW generator with chirp smoothing technique that is able to output linear FMCW frequency chirp using a nonlinear reference chirp signal supplied from a low spec/cost digital-oriented frequency reference is applied. The fabricated IC consists of an LNA, a down-conversion mixer with an output buffer, a driver amplifier, a power amplifier with power combiner, an LO distributer and an FMCW synthesizer. The measured FMCW signal from the proposed FMCW generator achieves 93 kHz frequency error (nonlinearity) at the 77 GHz chip signal. Radar performance of the IC has less than 1% ranging error from 1 m to 8 m distance from the measurement in a laboratory. These results show the transceiver achieves a fundamental function for radar applications with 520 mW power consumptions.**

***Index Terms*—Chirp radar, CMOS integrated circuits, FMCW, millimeter wave circuits, transceiver, 77 GHz circuits.**

I. Introduction

A 77 GHz radar application is suitable for measuring distance for various purposes owing to its narrow beam radius. In order to realize consumer radar/ranging applications for Intelligent Transportation System (ITS), a low-cost 77 GHz transceiver (TRX) is desired. A TRX using low-cost standard CMOS process instead of compound semiconductor or Si-Ge BiCMOS process is expected to be one of solutions capable of satisfying this demand in view of its suitability for high integration such as system-on-a-chip and the possibility of 77 GHz TRX in CMOS technologies is shown in recent research [1]–[3].

There are several ranging methods such as a pulse-radar, UWB radar and a frequency modulated continuous-wave (FMCW) radar [4]–[6]. Pulse radar and UWB radar require high peak-to-average power ratio (PAPR) or wideband operation to output short pulse signal or wideband spread spectrum signal. It is serious issue to manage with CMOS technology because the CMOS, unlike a compound semiconductor or a Si-Ge BiCMOS process, cannot be applied high supply voltage for obtaining high-power output signal and also it has lower maximum available gain (MAG) at millimeter-wave band for achieving wideband operation. On the other hand, the FMCW radars, that use only frequency modulation, require lower PAPR and moderate bandwidth than those required by other ranging methods. Therefore, the FMCW radar is a possible candidate for realizing a CMOS radar IC.

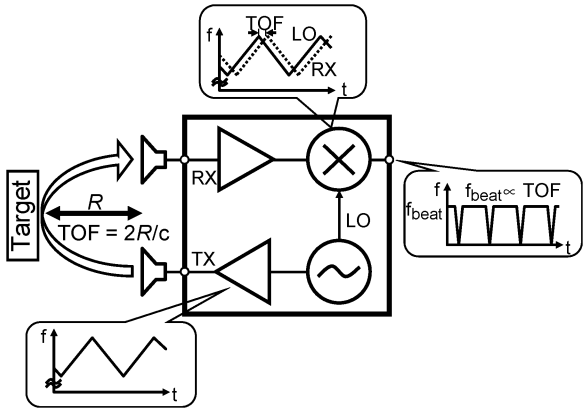


Fig. 1. FMCW radar transceiver.

Fig. 1 shows an FMCW radar TRX. An FMCW signal whose frequency is modulated in a triangular shape with time is generated by an FMCW signal generator. A transmitter (TX) amplifies the FMCW signal and radiates the signal via a TX antenna. Then, the radiated signal reaches the target located at a distance R from the TRX and the target reflects a portion of the signal back to the radar TRX. The reflected signal is input to the receiver (RX) via an RX antenna. The received signal is amplified and mixed with a local oscillation (LO) signal generated from the same FMCW generator used for the TX. Since the round-trip time of flight (TOF) of the signal is $2R/\mathrm{c}$, where c is the speed of light, the frequency difference between the received signal and the LO signal, which results in the frequency of the mixer output (f_{beat}), is related to the TOF (Fig. 1). Then, the distance can be obtained by frequency detection such as a fast Fourier transform (fft). Since the frequency difference is determined by a frequency chirp ratio of the FMCW signal, a highly linear frequency chirp is required to avoid degradation of ranging accuracy [7].

The first 77 GHz FMCW radar TRX IC fabricated in 90 nm CMOS process that applies a phase-locked-loop (PLL)-based

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T. Mitomo, N. Ono, H. Hoshino, O. Watanabe, and I. Seto are with the Wireless System Laboratory, Corporate Research and Development Center, Toshiba Corporation, Saiwai-ku, Kawasaki 212-8582, Japan (e-mail: toshiya.mitomo@toshiba.co.jp).

Y. Yoshihara is with the Advanced Circuit Design Department, Center for Semiconductor Research and Development, Semiconductor Company, Toshiba Corporation, Saiwai-ku, Kawasaki 212-0013, Japan.

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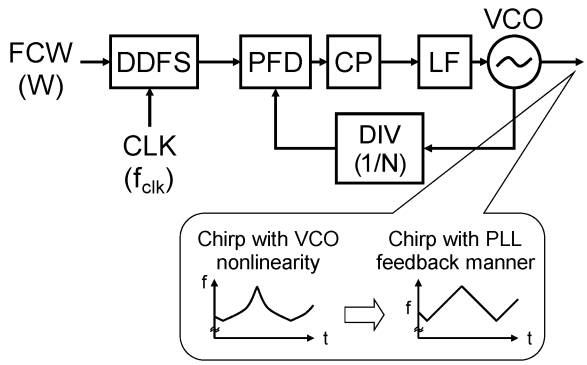


Fig. 2. Chirp linearization using a PLL with DDFS frequency reference.

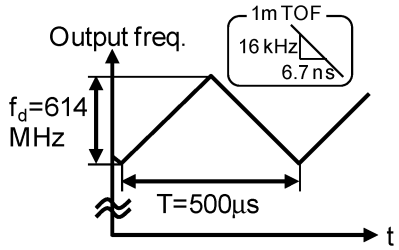


Fig. 3. Specification of an FMCW output frequency.

linear FMCW generator is presented [8]. This paper is organized as follows. Section II identifies design issues concerning realization of linear FMCW signal in CMOS IC and shows a proposed low-cost and low-power-consumption FMCW generator and results of numerical analysis. The design of the developed 77 GHz receiver and transmitter is presented in Section III, which is followed by the presentation of TRX measured results in Section IV. Conclusions are presented in Section V, the final section of this paper.

II. 77 GHz FMCW Signal Generator

A. Issues Concerning a CMOS IC for FMCW TRXs

In general, a 77 GHz voltage-controlled-oscillator (VCO) in CMOS is nonlinear with respect to the input frequency control signal owing to nonlinear devices such as a varactor diode of the VCO. A look-up table-based nonlinearity compensator for the VCO achieves linear frequency sweep. However the look-up table should be refreshed for the frequency drift with a temperature variation or other disturbance and the method cannot compensate fast frequency variation caused by unwanted load variation or disturbance. Delay line-based compensator generates linear frequency sweep by picking up the frequency variation ratio using a delay line and a mixer [9]. However, long delay line, which is hard to integrate in CMOS IC, is needed.

In the CMOS 77 GHz radar TRX, the PLL-based FMCW signal generator is used because a PLL can compensate the VCO nonlinearity by its feedback manner. A PLL using low frequency and accurate chirp FMCW reference signal generated by a direct digital frequency synthesizer (DDFS) is suitable for CMOS because the DDFS can be integrated in CMOS IC [10], [11]. Fig. 2 shows the block diagram of the PLL-based FMCW generator. Phase frequency detector (PFD) detects the phase/frequency difference between the output signal and reference signal, charge pump (CP) outputs source and drain current according to the polarity of the output of the PFD, the loop filter (LF) filters out the high frequency components and divider (DIV) output the frequency divided signal of the VCO output. The nonlinearity of the CMOS VCO is compensated by locking with an accurate frequency reference signal from the DDFS.

The frequency chirp of the reference signal has discrete stair-like shape. Required performances of the DDFS, such as clock frequency $(f_{\rm clk})$ and frequency control word length (W) corresponding to the phase resolution, can be determined by the refresh time of the frequency variation and the minimum frequency step. Fig. 3 shows a specification of the FMCW frequency chirp. In the case that the required ranging accuracy is 1 m, which corresponds to the TOF of 6.7 ns, the output frequency should change in 6.7 ns and the frequency variation in this time is 16 kHz. With regard to the reference signal, the DDFS should also change the output frequency in 6.7 ns. Hence, the minimum $f_{\rm clk}$ should be higher than 150 MHz. And this means the maximum output frequency of the DDFS is 75 MHz, which is equal to the Nyquist frequency of the $f_{\rm clk}$. In order to divide the 77 GHz output signal into 75 MHz reference frequency, the division number of the PLL is assumed to be 1024. This results in the required frequency resolution for the DDFS of less than 16 Hz.

Since the frequency resolution of the DDFS is determined by $f_{\rm clk}/2^W$, both 150 MHz $f_{\rm clk}$ and 24 bit W are needed for the FMCW frequency reference signal for the PLL. Such a high-speed and high-resolution DDFS requires high-power consumption over 100 mW and 1 mm^2 area including digital to analog converter (DAC) for DDFS output [12], [13]. Thus, a PLL that generates a linear FMCW signal even using a rough and low-resolution discrete stair-like frequency reference signal generated from low-spec DDFS that can be easily achieved in CMOS is desired to realize low-cost FMCW TRX for commercial radar applications.

B. Design of a CMOS FMCW Generator

Fig. 4 shows the proposed PLL for the FMCW radar. Rough stair-like time-domain frequency variation from the low-spec DDFS is converted to the time-domain voltage variation at the output of the charge pump of the PLL. Therefore, the low-pass loop filter (LF) can smooth the stair-like voltage variation, and the non-stair-like voltage signal is supplied to the VCO. Then, the output frequency variation of the PLL is smoothed into linear chirp. As shown in Fig. 4, a cut-off frequency of the PLL transfer function $(f_{\rm PLL})$ should be lower than $1/\Delta t$, which is the refresh rate of the low-spec DDFS, to suppress the spurs at $1/\Delta t$ that cause sinusoidal nonlinear frequency chirp at the output. The $f_{\rm PLL}$ should also be much higher than $1/T$ to create a triangular shape for FMCW signal. Therefore, a linear FMCW chirp signal can be generated by satisfying the inequality, $1/T \ll f_{\rm PLL} < 1/\Delta t$. For further relaxation of $f_{\rm clk}$ and W of the DDFS, the reference signal is generated from a single-sideband mixer and a CW signal generator (crystal oscillator) as shown in Fig. 4.

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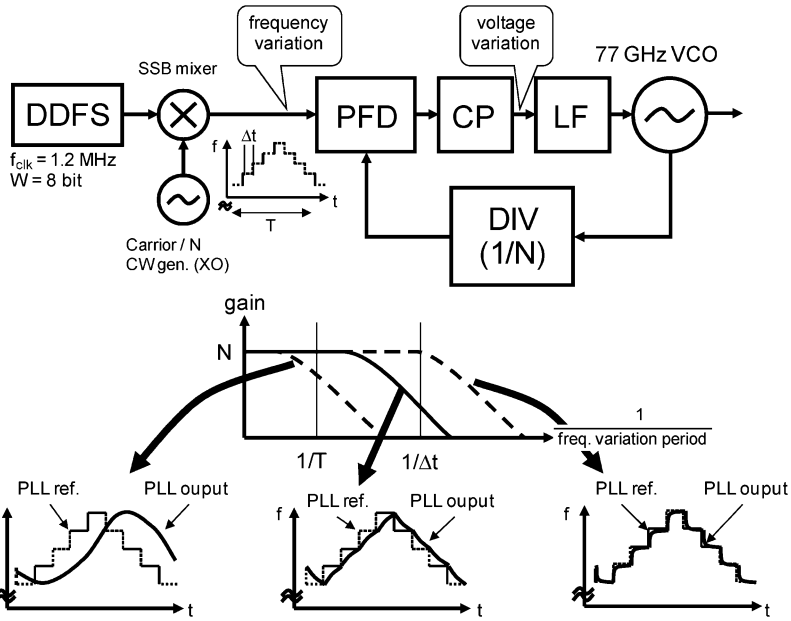


Fig. 4. Block diagram of the proposed PLL-based FMCW generator.

TABLE I
SPECIFICATIONS OF THE DDFS AND PLL

DDFS specification				
fclk	W	Δt	Freq. variation in Δt	6 kHz / 2.5 μs
1.2 MHz	8 bit	2.5 μs	6 kHz	

PLL specification					
LF type	LF capacitance	LF resistance	CP current	VCO Kv	N
Rag-filter	200 pF	15 kΩ	160 μA	1 GHz/V	1024

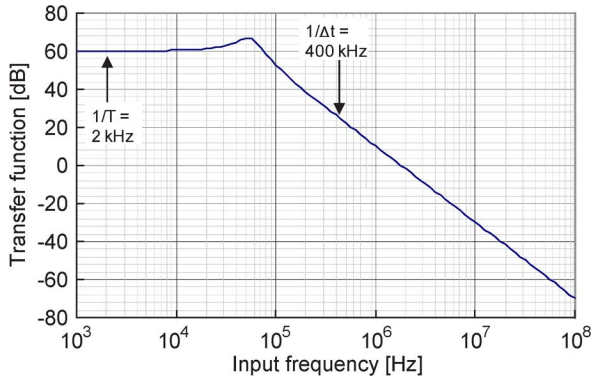


Fig. 5. Calculated transfer function of the PLL.

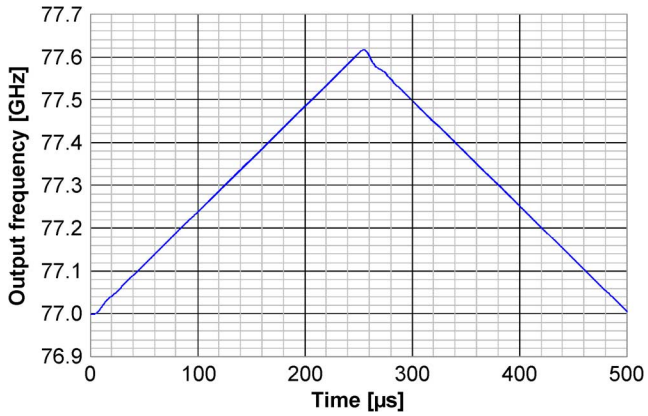


Fig. 6. Calculated FMCW output chirp of the proposed FMCW generator with low-spec DDFS.

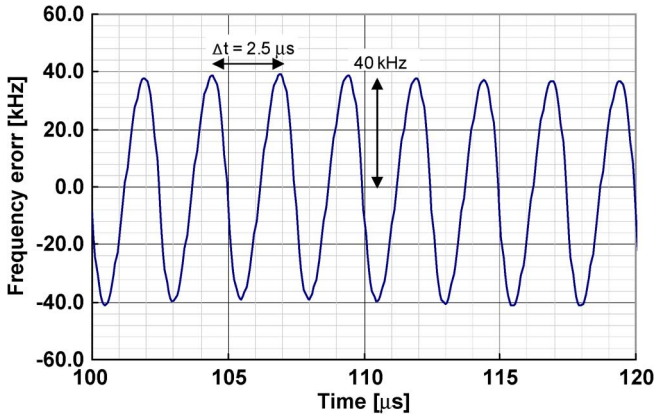


Fig. 7. Calculated frequency error of the proposed FMCW generator with 1.2 MHz, 8 bit DDFS for the frequency reference.

The output chirp linearity of the proposed PLL with low-spec DDFS for the frequency reference signal is estimated by using the parameters shown in Table I. Such a low-speed (1.2 MHz) and low-resolution (8 bit) DDFS consumes less than 1/10 power than that shown in Section II-A. The transfer function of the actual designed PLL calculated from parameters of VCO gain, LF characteristics, CP current and division number of DIV is shown in Fig. 5. The frequency component corresponding to the $1/\Delta t$ is suppressed by 30 dB and the $1/T$ is not suppressed by the PLL. The calculated output chirp of the PLL is shown in Fig. 6. Though the chirp overshoots at the turning point of the triangular

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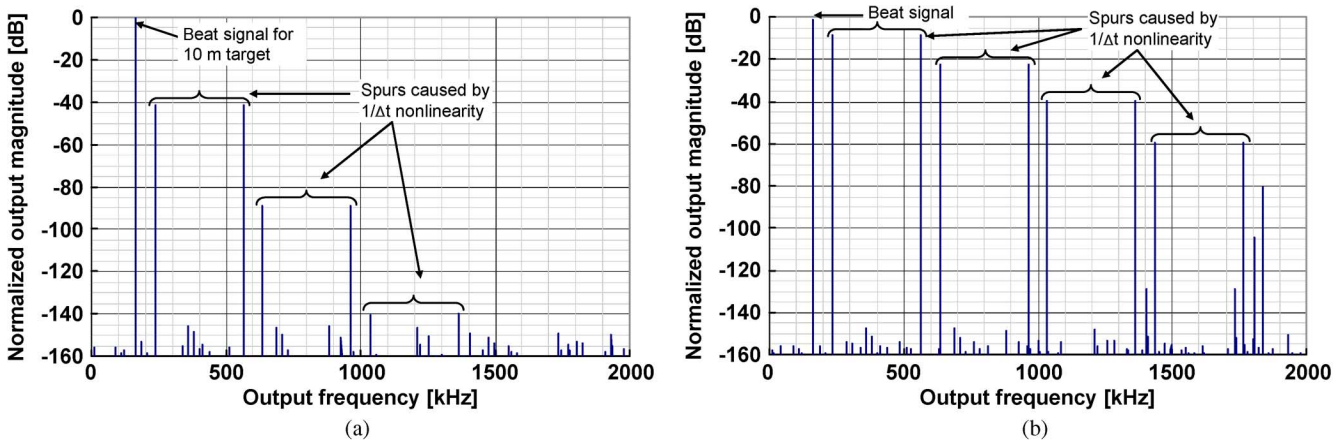


Fig. 8. Calculated radar output spectrum for a target located 10 m using the proposed FMCW generator (a) with smoothing function and (b) without smoothing function.

shape, the transition time is not long and the time can be neglected at the received signal processing. The output frequency error of the chirp is shown in Fig. 7. The chirp has sinusoidal nonlinearity whose error amplitude is 40 kHz at 77 GHz output. An FMCW radar output signal that has sinusoidal nonlinearity is

$$s_b(t)=c_0\cos 2\pi\left[\left(f_c+\frac{f_d}{2}\right)\mathrm{TOF}+\frac{f_d}{2T}(\mathrm{TOF})^2-\frac{f_d}{T}\mathrm{TOF}t+\frac{A_n\Delta t}{2\pi}\left\{\cos 2\pi\Delta t^{-1}(t-\mathrm{TOF})-\cos 2\pi\Delta t^{-1}t\right\}\right] \quad (1)$$

where c_0 is the amplitude of beat signal, f_c is the carrier frequency of the FMCW signal, f_d is the frequency deviation of the chirp and A_n is the magnitude of the sinusoidal nonlinearity (peak of the spurs at $1/\Delta t$) [7]. Fig. 8(a) shows the calculated radar output signal using (1) for a target at 10 m. The spurs that appear at $f_{beat}\pm 1/\Delta t$ are suppressed to 40 dB lower than desired beat signal at f_{beat}. The ranging resolution (standard deviation $\sigma_{\delta R}$) is also calculated from sinusoidal nonlinearity magnitude as [14]

$$\sigma_{\delta R}\approx\frac{\sqrt{2}A_n 1/\Delta t}{f_d/T\cdot c}R. \quad (2)$$

The result shows 46 cm resolution can be obtained for $R=100$ m. If the PLL does not have a smoothing function, the output chirp has very large, 3 MHz, error magnitude and the radar output signal for the same target becomes as shown in Fig. 8(b). The spurs are 30 dB larger than the previous case and the resolution is much more degraded.

III. TRX Building Blocks

The RX consists of an LNA, a down-conversion mixer and an output transimpedance and buffer amplifier as shown in Fig. 9. An LNA is needed to have sufficient gain for the receiver. However, nMOS transistors which we used have MAG of about 4 to 5 dB at 77 GHz, which is not sufficient to achieve desired gain with single stage amplifier. Furthermore, insertion loss of the passive components such as transmission lines (TLs) degrades the amplifiers gain. Thus, the LNA has five cascade amplifiers to achieve sufficient gain as shown in Fig. 10(a). Each cascade

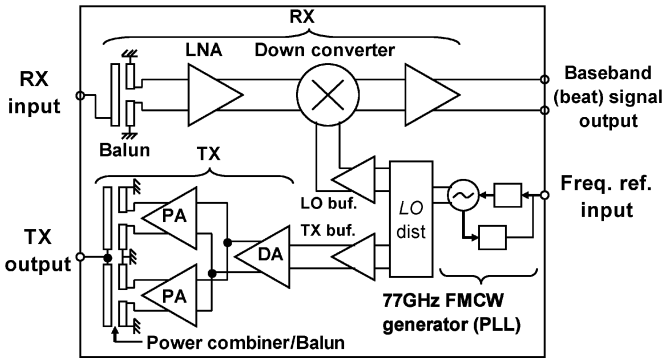


Fig. 9. Block diagram of the fabricated TRX IC.

amplifier has grounded coplanar TLs used as matching and load circuits both to avoid influences of lossy substrate and to suppress leakage signals from the TX circuit on the same die. As explained before, the IC is fabricated by using a standard CMOS process which does not have special thick copper layer. Therefore, a top aluminum layer for pads is used for the signal line to achieve lower insertion loss and 50 Ω characteristic impedance (Z_0). The insertion loss of the TL at 77 GHz is about 1.4 dB/mm in our design.

The LNA employs differential circuitry to avoid the influence of the complicated parasitic element networks at the ground and common nodes such as a power/bias supply [15] and each amplifier's input and output differential impedance is matched to 100 Ω. In order to obtain higher gain with lower current consumptions, a bias current density per gate width of the transistors is selected to 250 μA/μm which can obtain highest MAG of the nMOS transistors from the measured results. Since a general high gain/narrow beam antenna for radar applications is a single-ended input and output terminal, an on-chip TL-based Marchand balun is used at the input of the LNA to convert a single-ended signal from the 50 Ω output impedance of antenna to a differential signal of 100 Ω LNA input. The measured gains of the LNA with and without balun are 14 dB and 16.3 dB, respectively. The current consumption of the LNA is 45 mA.

A down-conversion mixer consists of a double-balanced mixer using a common-gate circuit for the input stage to obtain wider

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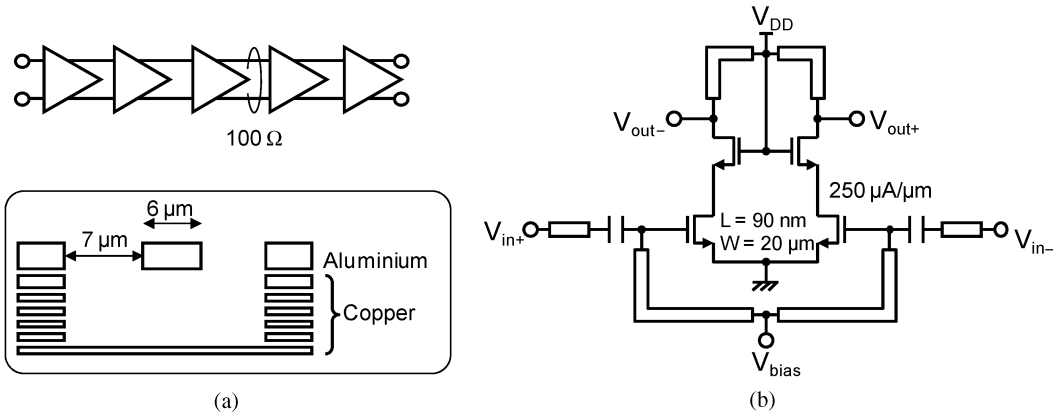


Fig. 10. The transmission line structure (a) and the LNA single stage circuit (b).

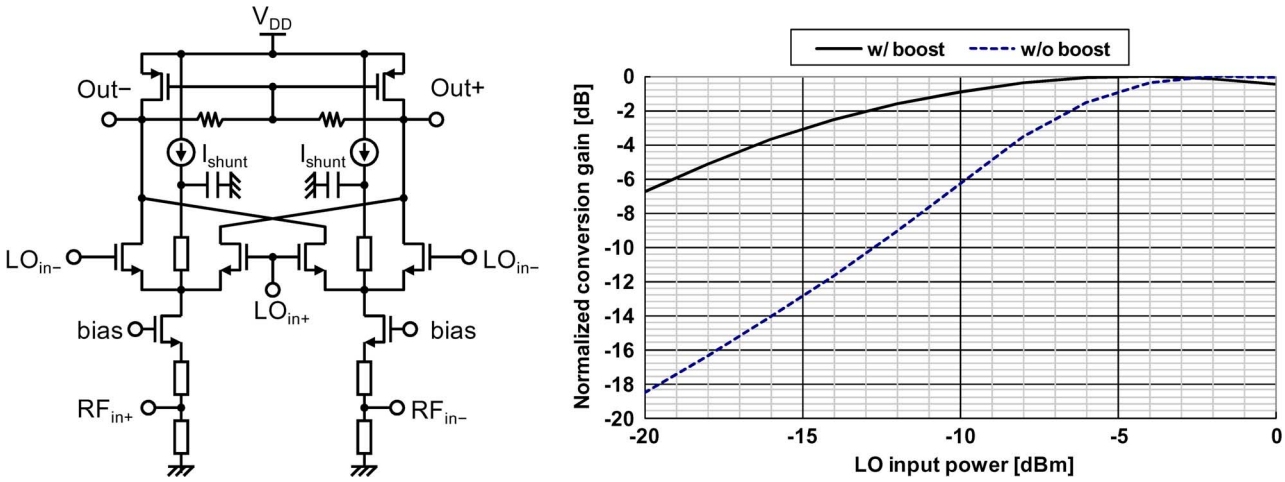


Fig. 11. Mixer circuit and conversion gain variation with LO input power.

bandwidth as shown in Fig. 11. The common source node of the switching pair of the mixer is connected to a current source to drive the switching pairs easily with small LO signal amplitude. The output power of the synthesizer is estimated about −12 dBm from the measured result and the power gain of the LO distribution circuit with two-stage common-source buffer amplifier is 2 dB from the simulation result. Thus, the LO input power for the down-conversion mixer (including a single stage LO buffer amplifier) is assumed to be around −10 dBm. Fig. 11 shows the simulated results of the normalized conversion gain variation with LO input power. The conversion gain with current source (boost) is saturated around −10 dBm LO input power which is much lower than the case without boost. TLs (inductances) are connected between the common-source of the switching pair and the current source in order to cancel the parasitic capacitances to achieve higher conversion gain [15].

The TX block has a power amplifier (PA) and a driver amplifier (DA) as shown in Fig. 9. Fig. 12 shows the PA consists of 2 differential common-source amplifiers and a power combiner. The Marchand balun based power combiner, which consists of $\lambda/4$ of the 77 GHz signal length TL based coupling line, is used to achieve differential to single-ended transformation, power combining of two amplifiers output and impedance transformation from the PA output impedance to 50 Ω for external antenna input impedance [17]. Fig. 12 shows the structure of the Marchand balun based power combiner. The output of the single-ended signal of each balun is in-phase. As a result, the output power of the combiner is ideally equals to twice the power of each PA. In order to obtain required coupling factor for the balun, the secondary line is placed between two primary lines as shown in Fig. 12. The architecture of the DA is the same as that of the LNA circuit to achieve sufficient gain from the synthesizer output and LO distribution circuitry.

A 77 GHz VCO consists of an nMOS cross-coupled pair with a resonator using a TL and accumulation-mode varactors. As shown in Fig. 13, wider metal compared to the 50 Ω TL used for other circuit blocks is applied to reduce insertion loss and to achieve higher Q. The TL has 38 Ω Z_0, 120 μm length. Since the TL is connected between the differential output nodes, the TL works as an inductor whose inductance is about 30 pH. The resonating capacitance including the parasitic capacitances at the output nodes is designed to have the value from 135 fF to 145 fF and the resonance frequency is designed to have around 77 GHz with 1 GHz variation under the control voltage from 0.2 V to 1.0 V. A prescaler for 77 GHz is an injection-locked frequency divider [15], [16]. Measured PLL locking range is about 800 MHz around 78 GHz and the phase noise is −85 dBc/Hz at 1 MHz offset as shown in Fig. 13.

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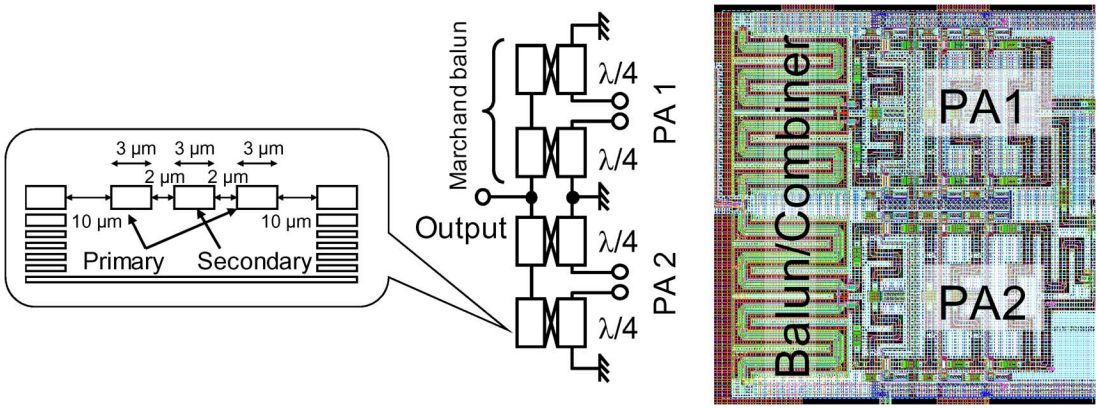


Fig. 12. The PA block diagram and layout image using a Marchand balun-based power combiner.

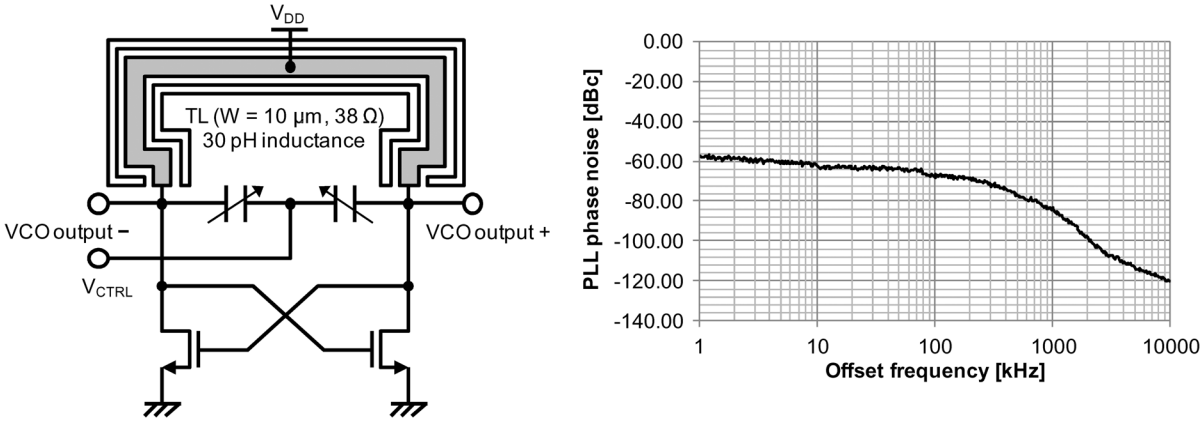


Fig. 13. The VCO circuit and the measured PLL phase noise.

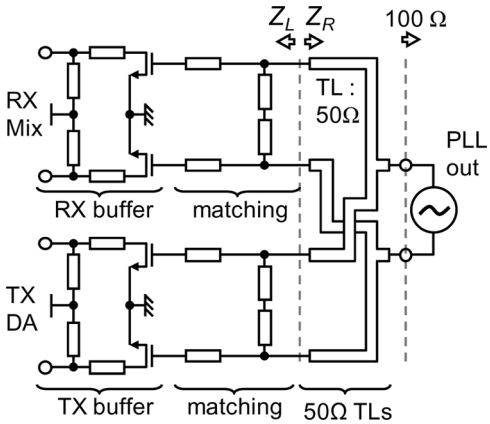


Fig. 14. Signal distribution for the TX and the RX buffers using simple power divider and distributor bsed-on transmission lines.

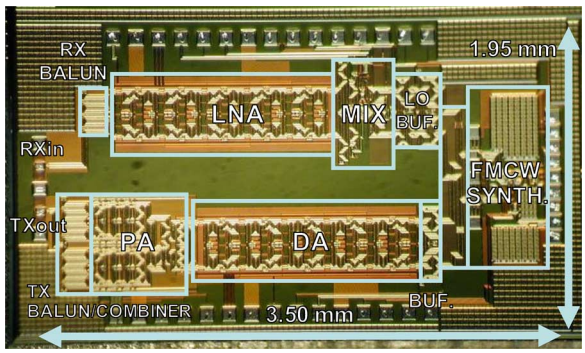


Fig. 15. Micro-photograph of the fablicated radar transceiver IC in a 90 nm CMOS process.

The output signal from the PLL is distributed to both the RX LO buffer connected to the mixer and the TX buffer amplifier connected to the DA. Fig. 14 shows the distribution network. The buffer amplifiers are connected to the PLL simply via TLs with $Z_0 = 50\ \Omega$ to reduce chip area and insertion losses. Since the RX and TX buffer circuits are the same architecture, the impedance matching and accurate power distribution are achieved simultaneously using the same matching circuit and distribution TLs.

IV. Measured Results

Fig. 15 shows a die photograph of the fabricated radar TRX IC using 90 nm CMOS process. The chip size including pads is $3.50 \times 1.95\ \text{mm}^2$. The fabricated IC is measured on a probe station and the frequency reference signal for the on-chip PLL is generated by using an arbitrary waveform generator as shown in Fig. 16. The frequency reference signal that is assumed to be an 8 bit/1.2 MHz DDFS is generated and the signal is converted to analog signal by 8 bit DAC. The output signal of the DAC is up-converted to 77 MHz carrier signal using SSB mixer and 77 MHz CW signal. The measured output spectrum of the

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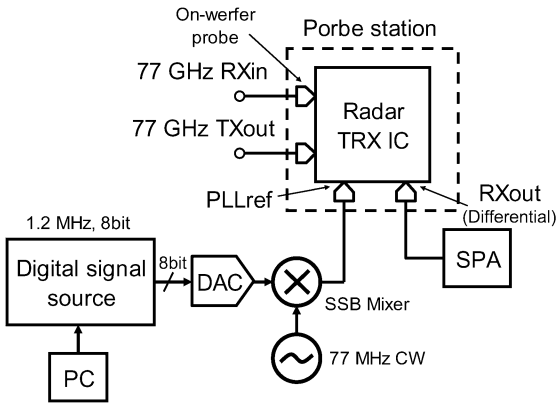


Fig. 16. Measurement setup of the radar transceiver IC.

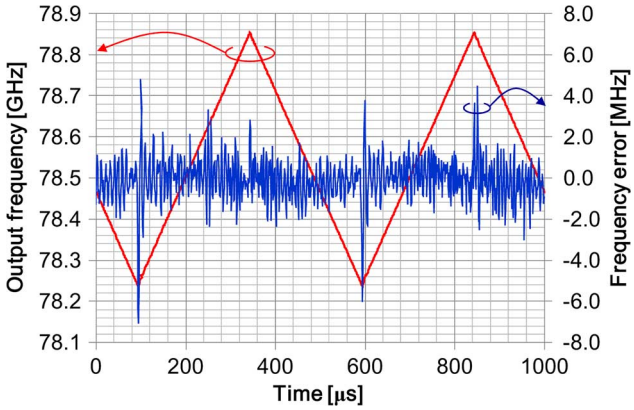


Fig. 18. Measured output frequency chirp and time-domain frequency error to an ideal FMCW chirp.

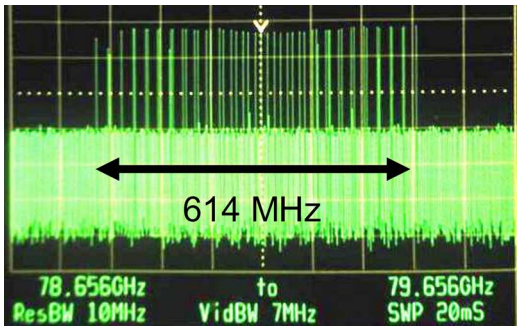


Fig. 17. Radar measurement using a external antenna and fabricated radar transceiver IC.

TX is shown in Fig. 17. The spectrum that has 614 MHz bandwidth is achieved from a 600 kHz bandwidth frequency reference signal and $N = 1024$ division PLL. Note that the Fig. 17 is a photograph of the display of the spectrum analyzer. Although the measurement was done by 20 ms sweep time that is shorter than FMCW chirp period, the image of previous sweeps is remained. Therefore, the spacing of the spectrums in Fig. 17 is not uniform.

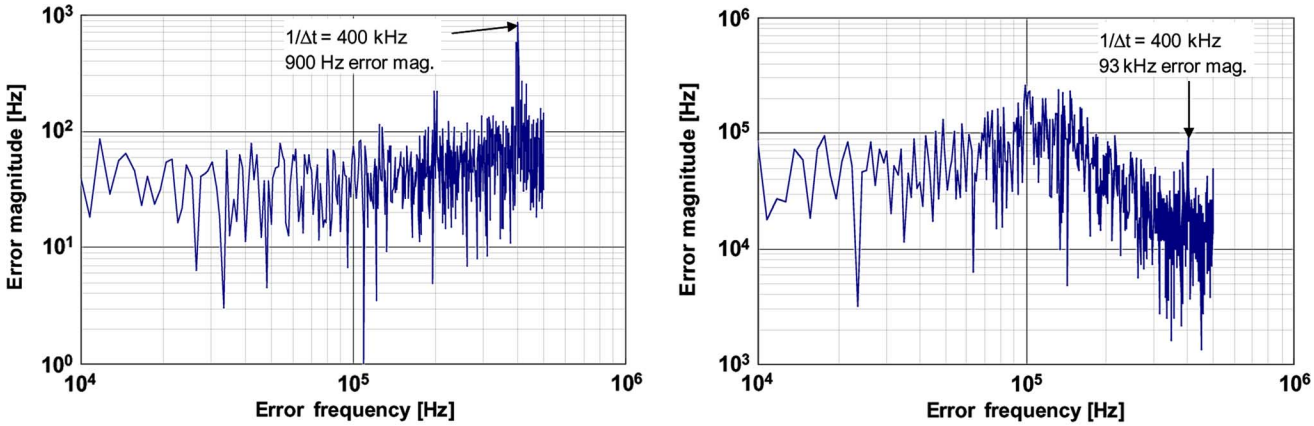
Frequency chirp is also measured by using an external down-conversion mixer and a signal source analyzer. Fig. 18 shows a measured time-domain frequency chirp of the TX output. The result shows a linear frequency chirp is achieved even using a low-spec rough stair-like frequency reference signal. The FMCW frequency error (sinusoidal nonlinearity) is extracted by subtraction of an ideal FMCW frequency chirp from measured FMCW frequency chirp. The time-domain frequency error is shown in Fig. 18, indicating that the standard deviation of the error magnitude of 1.05 MHz appears at any time. In order to extract sinusoidal nonlinearity from the measured results, the time domain frequency error variation is converted to frequency domain by using fft. Fig. 19(a) shows the output frequency error at the reference signal in frequency domain. Large spur appears at 400 kHz, which is equal to $1/\Delta t$, caused by stair-like frequency chirp from low-spec DDFS. Since the phase noise of the arbitrary waveform generator is not sufficiently low, the frequency reference signal has flat frequency error like white noise. This results in large frequency error at the transmitted signal as shown in Fig. 18. The noise can be reduced by using more accurate low-frequency DAC for the DDFS output and low phase noise CW generator such as a crystal oscillator. Fig. 19(b) shows the frequency domain error magnitude of the transmitted signal. Even though the white noise in the reference signal is multiplied 1024 times, the spur at $1/\Delta t$ is suppressed by using the proposed PLL. The sinusoidal error magnitude that corresponds to the magnitude of the spur at $1/\Delta t$ is 93 kHz. According to (2), the ranging resolution is about 1 m for a target located at 100 m distance. Note that the cut-off frequency and the peaking property of the PLL transfer function of the fabricated IC is not same to the estimated result as shown in Fig. 5 due to variation of the loop filter components (resistance and capacitance) and the CP current.

Ranging performance of the fabricated TRX IC is measured by using external 20 dBi horn antennas. Ranging measurement for the fixed target is done with the setup as shown in Fig. 20. The output signal of the TRX is radiated to the ceiling at 2.8 m distance and the reflected signal is input to the receiver antenna. Fig. 21 shows a spectrum of the received signal. The peak of the spectrum is located at 46 kHz, which corresponds to 2.8 m for the fabricated FMCW radar. Spurs at 46 kHz $\pm$ 400 kHz $(1/\Delta t)$ arise owing to the nonlinearity of the FMCW frequency chirp is less than 30 dB (the same level as the floor noise). Note that the spectrum around 86 kHz is double-reflected signal by the probe station. The distance for 86 kHz is shorter than 2.8 m $\times$ 2 because the path does not include the cable between the antenna and the IC in the first reflection path.

The radar performance is also measured using a small metal reflector target with various distances and the measured distance is shown in Fig. 22. The standard deviation of the error for each measurement is less than 1% for a target at from 1 m to 8 m. Note that we have no velocity data because we do not have a moving target.

The performance of the 77 GHz TRX is summarized in Table II. A ranging distance with a certain detection probability and false alarm ratio can be estimated by signal-to-noise

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(a) (b)

Fig. 19. Measured frequency domain frequency chirp error against an ideal FMCW signal of (a) the frequency reference and (b) the output signal.

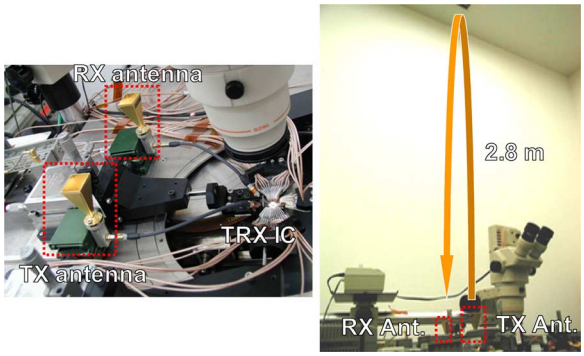


Fig. 20. Radar measurement using an external antenna and fabricated radar transceiver IC.

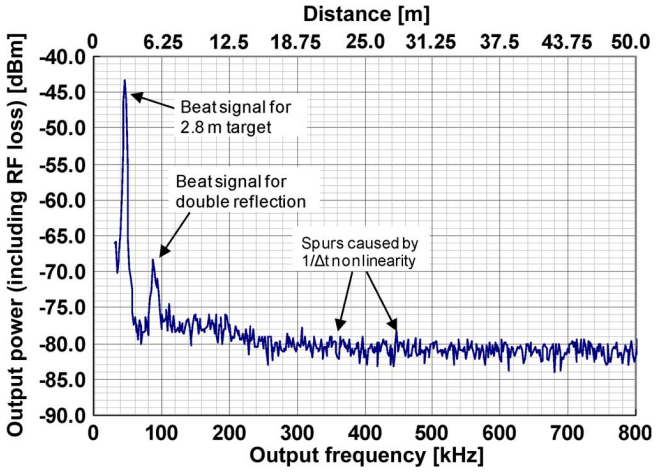


Fig. 21. Measured output spectrum that is corresponding to the target distance for the target located at 2.8 m.

ratio (SNR) of the received signal [4]. The received power is estimated from the radar equation [4]

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{3}$$

where P_t is the output power of the TX, G_t and G_r is the antenna gain for input and output, λ is the wavelength of the 77 GHz

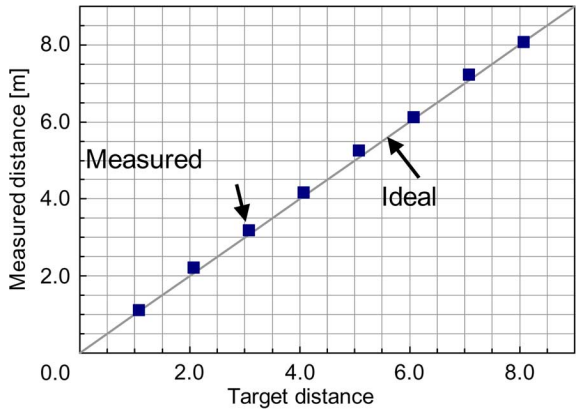


Fig. 22. Measured distance for a target located 1 m to 8 m distance.

TABLE II
PERFORMANCES OF THE RADAR TRANSCEIVER IC

Synthesizer operating frequency	[GHz]	78.1−78.8
Synthesizer output power	[dBm]	−13
Synthersizer phase noise (1MHz offset)	[dBc/Hz]	−85
Synthesizer power consumption (1.2V Supply)	[mW]	101
TX ouput power	[dBm]	−2.8
TX power gain	[dB]	14
TX power consumption (1.2V Supply)	[mW]	305
RX power gain	[dB]	23.1
RX noise figure (single side band)	[dB]	15.6
RX power consumption (1.2V Supply)	[mW]	111

signal and σ is the reflection cross section of target. The SNR is calculated from the received power at the RX input, noise figure of the RX and the resolution of the fft at baseband DSP. The receiver SNR ($\mathrm{SN_{RX}}$) in ideal environment is calculated by

$$\mathrm{SN_{RX}} = \frac{P_r}{\kappa T \cdot \mathrm{NF} \cdot f_{\mathrm{fft}}/p_{\mathrm{fft}}}. \tag{4}$$

For achieving the detection probability of 99% and the false alarm ratio of 10^{-10}, 16 dB of $\mathrm{SN_{RX}}$ is required [4]. In order to estimate the $\mathrm{SN_{RX}}$ of the fabricated TRX IC, the parameters in Table III are used for the variables in (3) and (4) and σ of 10 m^2 is used assuming a small car target [18], [19]. The calculated

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TABLE III
ESTIMATED LINK-BUDGET OF THE FABRICATED IC

PA output power	P_t	[dBm]	-2.8
TX antenna gain	G_t	[dBi]	20
RX antenna gain	G_r	[dBi]	20
Wave length	λ	[mm]	3.9
Reflection cross section	σ	[m^2]	10
Distance	R	[m]	107
Receiver NF	NF	[dB]	15.6
fft Nyquist freq.	f_{fft}	[MHz]	2.0
fft points	p_{fft}		4096
RX Input noise	κT	[dBm/Hz]	-173.8
RX Input power	P_r	[dBm]	-115.1
RX S/N	SN_{RX}	[dB]	16.17

result shows 16 dB $\mathrm{SN_{RX}}$ is obtained for $R = 107$ m. Note that the fft period is longer than that of FMCW chirp (4096 points for 2 MHz Nyquist frequency) in order not to degrade the $\mathrm{SN_{RX}}$ from fft resolution.

V. CONCLUSION

The first CMOS radar TRX IC using a PLL capable of generating linear FMCW frequency chirp with low-spec DDFS is presented. The transceiver employs a PLL capable of smoothing nonlinear stair-like reference frequency signal generated by low-spec DDFS. The measured results show that the chirp nonlinearity of the output signal from the transmitter is 93 kHz for 614 MHz bandwidth with 77 GHz band carrier. The fabricated IC shows less than 1% ranging error for 1 m to 8 m ranging measurement and the estimated maximum ranging distance for 10 m^2 (small car) reflection cross section target in ideal condition is 107 m. These measured results show the TRX IC achieves fundamental performance for FMCW radar applications.

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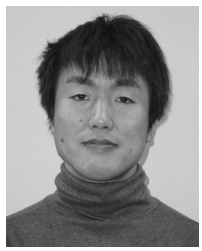
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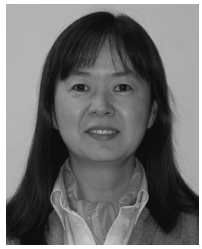
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Toshiya Mitomo (M'09) received the B.E. degree from the Science University of Tokyo, Tokyo, Japan, in 2000 and the M.E. degree from the Tokyo Institute of Technology in 2002.

He joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2002. Since then, he has been engaged in research and development of wireless communication circuits.

Mr. Mitomo is a member of the Institute of Electrical, Information and Communication Engineers (IEICE).



Naoko Ono was born in Tokyo, Japan. She received the B.E. and Ph.D. degrees in electrical engineering from the Science University of Tokyo, Japan, in 1991 and 2004, respectively.

She joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 1991, where she has been engaged in the research and development of high-frequency analog circuit designs, such as V-band monolithic GaAs HEMT amplifiers and millimeter-wave CMOS ICs.

Dr. Ono was a recipient of the 2001 Young Engineer Award from the Institute of Electrical, Information and Communication Engineers (IEICE).

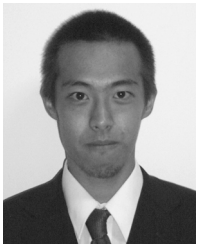
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Hiroaki Hoshino received the B.E. and M.E. degrees in communications and computer engineering from the Graduate School of Informatics, Kyoto University, Kyoto, Japan, in 2001 and 2003, respectively.

He joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2003. Since then, he has been engaged in research and development of wireless communication circuits.

Mr. Hoshino is a member of the Institute of Electrical, Information and Communication Engineers (IEICE).



Yoshiaki Yoshihara (M'07) received the B.E. degree in electronical and electronics engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2003, and the M.E. degree from the Department of Advanced Applied Electronics, Tokyo Institute of Technology, Yokohama, Japan, in 2005.

In 2005, he joined Toshiba Corporation, where he is engaged in wireless circuit design with the Center for Semiconductor Research and Development.

Mr. Yoshihara is a member of the Institute of Electrical, Information and Communication Engineers (IEICE).



Osamu Watanabe (M'03) received the B.S. and M.S. degrees in physics from Tohoku University, Sendai, Japan, in 1993 and 1995, and the Doctor of Engineering degree from the Tokyo Institute of Technology, Tokyo, Japan, in 2008.

In 1995, he joined the Corporate Research and Development Center, Toshiba Corporation, Kanagawa, Japan. Since then, he has been engaged in research and development of wireless communication circuits.

Dr. Watanabe is a member of the Institute of Electrical, Information and Communication Engineers (IEICE).



Ichiro Seto (M'06) received the B.E. and M.E. degrees from Keio University, Kanagawa, Japan, in 1991 and 1993, respectively.

In 1993, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he has been engaged in research and development of optical communication systems and wireless communication systems.

Mr. Seto is a member of the Institute of Electrical, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 2001 Young Engineer Award from the IEICE.

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